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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,133	03/26/2001	Hisao Suzuki	108075-00054	5889

7590

10/01/2003

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EXAMINER

TRA, ANH QUAN

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/816,133

Applicant(s)

SUZUKI ET AL.

Examiner

Quan Tra

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) 11-35 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-10 is/are allowed.
- 6) ☒ Claim(s) 1 and 36-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 09/08/2003. Applicant's arguments have been fully considered but they are not persuasive. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 36-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Okutsu et al. (USP 6433623) (newly cited).

As to claims 1 and 36, Okutsu et al. discloses in figure 1 a level shift circuit comprising : a capacitor (C1) ; a charge control circuit (P13) connected to the capacitor for providing a voltage of a high potential power supply (Vcc) to the capacitor and controlling charging of the capacitor; and a limiting circuit (P12) connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor, wherein the limiting circuit limits the voltage provided to the capacitor when boosting of an output signal (signal at node 9) of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Art Unit: 2816

As further called in for claim 36, figure 1 shows the charge control circuit comprises a first transistor (P13), and the limiting circuit comprises a second transistor (P12).

As to claim 37, figure 1 shows the second transistor is transistor is turned off by a control signal generated on the basis of an input signal (output of G9).

As to claim 38, figure 1 shows the second transistor is turned off when stepping up a voltage of an input signal (inherent).

As to claim 39, figure 1 shows the second transistor limits a flow of current from the capacitor to the high potential power supply.

As to claim 40, figure 1 shows the limiting circuit includes a transistor (P12).

As to claim 41, figure 1 shows transistor P12 is turned off when limiting the voltage provided to the capacitor.

As to claim 42, figure 1 shows the transistor (P12) limits a flow of current from the capacitor to the high potential power supply.

Claim 43 recites similar limitations of claims 1 and 36. Therefore, it is rejected with the same reasons.

Allowable Subject Matter

3. Claims 2-10 are allowed.

Response to Arguments

4. Applicant argues that “the limiting circuit limits the voltage provided to a capacitor from the high potential power supply voltage before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. That is, the limiting circuit is turned off before the charge control circuit is turned off”. The Examiner respectfully disagrees.

Nowhere in the claim recites “the limiting circuit is turned off before the charge control circuit is turned off”. Okutsu et al. shows transistor P12 and transistor P13 are simultaneously turned off. Therefore, transistor P12 limiting the current from Vcc to node 9 until transistor P 13 is turned off, thus limiting the current from Vcc to node 9 before transistor P13 is turned off.

Applicant further argues that “Okutsu also fails to disclose or suggest that the limiting circuit limits the voltage provided to the capacitor when boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply”. Figure 1 shows transistors P12 is turned off in boosted mode, thus limiting the current from Vcc to node 9.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Art Unit: 2816

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.


7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



QT
September 29, 2003


Terry D. Cunningham
Primary Examiner